Private Circuits Revisited:

Provable Security Guarantees on Boolean Circuits

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Gap in Provable Security

Approach in provable security
- Develop adversarial model
- Define what is understood under the security of algorithm
- Prove that no adversary can exist under reasonable assumptions
  ➔ prove security always against any adversary

Proof by simulation

Show that there exists a simulator that without the „secret“ can produce an outcome that is indistinguishable from „real world“. 

\[
\begin{align*}
A & \quad b = 0 \\
b & \quad R \{0, 1\} \\
b' = b?
\end{align*}
\]
Gap in Provable Security

Traditional Provable Security
- Cryptographic algorithms are modeled as black boxes
- Adversary may have access to inputs and outputs
- Inner workings during computation are not revealed

Gap to real-world implementations
- Physical devices do not behave as black-boxes
- Adversary can take step outside of black box model and attack physical devices differently, e.g.:
  - Side-channel: partial view on the inner working of implementations
  - Tampering attacks: change inner workings of implementations

Rest of this talk...

1. Physical Security Models
2. Definitions
3. Circuit Transformation
4. Drawbacks in Practice
5. Ongoing Research
1. Physical Security Models

Close the gap in provable security

1. M&R Model: Model computation as Turing machine but augment it with leakage function to cover all possible leakages
   - Goal: Given PO secure building block $P_1$, can we build more complex constructions $P$?

2. ISW03 Model: Consider specific implementations and a particular adversarial model
   - Computing device: Only boolean circuits with very limited instruction set and memory
   - Adversarial Model: Adversary is „only“ allowed to probe $t$ wires
   - Goal: Construction where the adversary learns no additional information (e.g. content of memory) by probing $t$ wires (i.t.)
2. Definitions

Boolean circuit: Modelled as a tree
- Vertices are Boolean gates and edges are wires
- Circuit is evaluated on input in one clock cycle
- Random-bit gates: Outputs one random bit for each invocation
- Memory cell: One input, outputs for each invocation the previous input
  - stateless circuit: circuit contains no memory cells
  - stateful circuit: circuit contains memory cells

Equivalence of stateless circuit
\[ C \equiv C', \text{ if for inputs } x, C(x) \text{ and } C'(x) \text{ are identically distributed} \]

Stateless transformer (T,I,O):
- I: Input encoding
- T: Circuit core transformation
- O: Output decoding
2. Definitions

Properties of a Stateless Transformer (T,I,O)

- **Soundness:** For all C it holds that \( C \equiv O \circ T(C) \circ I \)

- **Privacy:** For every \( t \)-limited adversary \( A \) there exists a \( 0 \)-limited simulator \( S \), such that for every circuit \( C \) and every input \( x \), the output distribution of \( A \) and \( S \) are identically distributed.
  
  - A learns no new information by probing
  - Note: A tries to learn information on input/output of the circuit

3. Circuit Transformation

Theorem [ISW03]: There exists a \( t \)-private stateless transformer \((T,I,O)\) which maps any circuit \( C \) of size \( n \) to a randomized stateless circuit of size \( O(nt^2) \)

**Basic Idea:**

- Use additive secret sharing and split every input in \( t \) shares
- Replace every gate in \( C \) by a new (secure) gadget in \( C' \)
- Show for every input \( x \) to \( C \): \( \Pr[x = 1 | \text{Adversary probes } t \text{ wires}] = 1/2 \)
3. Circuit Transformation

Transformation (T,I,O):

- Input Encoding I: Input: x; Output: t+1 additive shares r₁,...,rᵣ of x
  - Choose t random bits: r₁,...,rᵣ
  - rᵣ₊₁ = x + r₁ + ... + rᵣ
- Output Decoding O: Input: t+1 shares of y; Output: y
  - y = y₁ + ... + yᵣ₊₁

Circuit Core Transformation T(C) (wlog C has only NOT and AND gates):

- Replace every wire w in C by t+1 wires carrying an (t+1,t+1) additive secret sharing of the value on w

- NOT gate on wire w: put NOT gate on wₙ
  
  w ← w₁ + w₂ + w₃
  \[ y_w = y_w₁ + y_w₂ + y_w₃ \]
3. Circuit Transformation

AND gate with inputs a, b and output c

Observe: \( c = ab = (a_1 + \ldots + a_{t+1}) (b_1 + \ldots + b_{t+1}) = a_1 b_1 + \ldots + a_{t+1} b_{t+1} \)

First attempt: \( c_i = a_i b_i + \ldots + a_{t+1} b_{t+1} = a_i (b_1 + \ldots + b_{t+1}) \)

- **Soundness:** \( c = c_1 + \ldots + c_{t+1} \)
- **Privacy:** No! Probing only one wire results in bias
  - Let \( t=3 \). Probing of \( c_1 = a_1 b \Rightarrow P[b = 1 | c_1 = 1] = 1 \neq \frac{1}{2} \)

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3. Circuit Transformation

AND gate with inputs a, b and output c

- **Compute intermediate values** \( z_{ij} \) for \( i \neq j \)
  - If \( 1 \leq i < j \leq t+1 \): Introduce a random bit gate \( z_{ij} \)
  - Else: \( z_{ij} = (z_{ji} + a_i b_j) + a_i b_i \)
- **Output of AND gate:** \( c_i = a_i b_i + z_{i1} + \ldots + z_{t+1} \)
- **Soundness:**
  - Observe: \( z_{ij} + z_{ji} = a_i b_j + a_j b_i \)

\[
\begin{array}{c|ccc}
   & a_i b_1 & z_{i2} & z_{i3} \\
\hline
   c_1 & a_1 b_1 & & \\
   c_2 & z_{21} & a_2 b_2 & z_{23} \\
   c_3 & z_{31} & z_{32} & a_3 b_3 \\
\end{array}
\]
3. Circuit Transformation

Privacy: For every $t$-limited adversary $A$ there exists a $0$-limited simulator $S$, such that for every circuit $C$ and every input $x$, the output distribution of $A$ and $S$ are identically distributed.

![Diagram](image)

Proof idea:

Further Results (Ishai et al.):

- More efficient constructions for statistic security
  - Statistic security: Small (but negligible) simulation error
  - Blow up of circuit size by only a factor of $t$, but the construction hides large constants $\Rightarrow$ only more efficient for large $t$
- More efficient constructions for a particular cryptographic scheme
  - Deterministic PRNG circuit with size $O(nt)$
  - The PRNG circuit can be used to replace the random bit gates in the general construction
4. Drawbacks in Practice

- Construction only of theoretical interest
  - Blow up by a factor of $t^2$. In practice doubling the circuit size is for many applications already too much. Security is not for free!
  - Every AND gate needs around $t^2$ bits of fresh randomness in each clock cycle
- Model does not consider relevant implementation details such as:
  - Glitches
  - Early propagation effect
- Probing is done by an invasive adversary, but in practice non-invasive attacks are more serious threat to security

4. Drawbacks in Practice

- Power Analysis model:
  - An adversary learns not the value on the wire but if the value on the wire has flipped
  - Non-invasive adversary obtains power consumption by measuring from outside
- Ishai construction in the power analysis model?
  - Perfect security cannot be achieved in power analysis model
  - Attack: all shares of an input can contribute to the measured power consumption at one moment. Measurement is correlated with secret input
5. Ongoing Work

- New model to analyze security of boolean circuits in power analysis model that incorporates:
  - Glitches,
  - Early propagation effect,
  - Memory effect,
  - ......  

\[ \text{Super-Model} \]

- Design new logic style that achieves some provable security but still has practical relevance
  - Small blow-up factor
  - Only few fresh randomness per clock cycle

RE-TRUST Meeting, St. Petersburg

Thank you for your attention!